AXM-VFX-EDK
Mezzanine Module

USER'S MANUAL

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TABLE OF CONTENTS

IMPORTANT SAFETY CONSIDERATIONS

You must consider the possible negative effects of power, wiring, component, sensor, or software failure in the design of any type of control or monitoring system. This is very important where property loss or human life is involved. It is important that you perform satisfactory overall system design and it is agreed between you and Acromag, that this is your responsibility.

1.0 General Information

2.0 PREPARATION FOR USE

3.0 PROGRAMMING INFORMATION

4.0 THEORY OF OPERATION

5.0 SERVICE AND REPAIR

6.0 SPECIFICATIONS

TABLE OF CONTENTS

DRAWINGS

1.0 GENERAL INFORMATION

The AXM-VFX-EDK board (sold with the PMC-VFX base boards' Engineering Design Kit) provides the standard Xilinx JTAG header, two RS232 terminal connections, as well as direct connections to the Xilinx FPGA. These general purpose LVTTL (Low Voltage TTL) I/O points allow the user to emulate AXM-D modules while using ChipScope®.

Table 1.1: *AXM-D Series and AXM-EDK Models*

MODEL	Front I/O Type	Front I/O Connector	OPERATING TEMPERATURE RANGE
AXM-VFX-EDK	JTAG & LVTTL & RS232	Xilinx Std JTAG & 34-Pin 0.1" Header & Two DP9	0°C to +70°C

KEY FEATURES

- **Digital Input/Output Channels** – Thirty 3.3 volt LVTTL/CMOS compliant input/output channels which can be configured as input or output with independent direction control.
- **Xilinx JTAG Interface** – The EDK board provides the standard Xilinx JTAG interface to allow direct programming of the FPGA and an interface with ChipScope®.
- **Two RS232 DP9 Ports–** The RS232 ports are provided for program data display and for general program debug and development.
- **Programmable Change of State/Level Interrupts –** Example code provides interrupts that are software programmable for any bit Change-Of-State or level on 8 channels.
- **Example Design –** The example VHDL design, provided in the base board EDK, includes control of all I/O, and eight Change-Of-State interrupts.

ENGINEERING DESIGN KIT

The AXM-VFX-EDK is included with the Engineering Design Kit of the PMC-VFX base board. The AXM-VFX-EDK board allows programming via the JTAG interface, program display and general program debug and development. Refer to the PMC base board's manual for further information on the available Engineering Design Kit.

BOARD CONTROL SOFTWARE

Acromag does not provide board control software specifically for the AXM-VFX-EDK. However, the AXM-VFX-EDK module can be accessed via the control software for the base PMC module. The AXM-VFX-EDK can be used withthe following operating systems: Windows® DLL, VxWorks®, and QNX®. Refer to the PMC base board's manual for further information.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation.

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

CARD CAGE CONSIDERATIONS

IMPORTANT: *Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.*

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the system boards, plus the installed Acromag board, within the voltage tolerances specified.

Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

Remove power from the system before installing board, cables, termination panels, and field wiring.

Default Hardware Configuration

The AXM-VFX-EDK cannot stand-alone and must be mated with a compatible Acromag PMC-VFX module. The default configuration of the control register bits at power-up is described in section 3.

Front Panel Field I/O Connector

The AXM-VFX-EDK board has four front I/O connectors. The first is a double row 14-pin 2mm header (male) for JTAG programming. This is the standard Xilinx JTAG Header. The second I/O interface is a double row 34-pin 0.1" header (male). A standard floppy drive cable can be used to connect to the interface. The third and fourth I/O interfaces are 9-pin DSUB right-angle female connectors. Note the cables are available from Acromag.

AXM-VFX-EDK Front I/O

The AXM-VFX-EDK has a standard 34 pin double row 0.1" header for front I/O. The I/O are LVTTL/CMOS compatible. These pin connections can emulate the 30 differential channels on the AXM-D02 and AXM-D04 models and the 22 differential channels on the AXM-D03 model using LVTTL signaling. Refer to the Differential I/O Register section for further information. Front I/O connections are listed in Table 2.1.

The AXM-VFX-EDK front I/O also includes the standard Xilinx 14-pin 2mm JTAG header. This header can be used to directly program the FPGA or to interface with the FPGA debug software ChipScope®. The pin connections are shown in table 2.2.

In addition, the AXM-VFX-EDK contains 12 auxiliary pins that are routed to two 8 pin SIP patterns on the board. *Note that these are not front panel I/O connections.* Due to height restrictions SIP sockets are not installed. This allows for full end user customization. These pins correspond to the 12 channels of Digital I/O on the AXM-D03 module. Refer to the Digital I/O Register section for further information. The connections are listed in table 2.3.

Lastly, the AXM-VFX-EDK contains two right angle 9-pin DSUB or DB9 sockets that are routed to two UARTs on the PMV-VFX board. The connections are listed in table 2.4.

Refer to drawing 4502-107, located at the end of this manual, for I/O pin locations on the AXM-VFX-EDK.

34-Pin Double Row 0.1" I/O Header			
Pin Description	**Pin**	**Pin Description**	**Pin**
COMMON	1	COMMON	2
LVTTL Channel 0	3	LVTTL Channel 1	4
LVTTL Channel 2	5	LVTTL Channel 3	6
LVTTL Channel 4	7	LVTTL Channel 5	8
LVTTL Channel 6	9	LVTTL Channel 7	10
LVTTL Channel 8	11	LVTTL Channel 9	12
LVTTL Channel 10	13	LVTTL Channel 11	14
LVTTL Channel 12	15	LVTTL Channel 13	16
LVTTL Channel 14	17	LVTTL Channel 15	18
LVTTL Channel 16	19	LVTTL Channel 17	20
LVTTL Channel 18	21	LVTTL Channel 19	22
LVTTL Channel 20	23	LVTTL Channel 21	24
LVTTL Channel 22	25	LVTTL Channel 23	26
LVTTL Channel 24	27	LVTTL Channel 25	28
LVTTL Channel 26	29	LVTTL Channel 27	30
LVTTL Channel 28	31	LVTTL Channel 29	32
COMMON	33	COMMON	34

Table 2.1: AXM-VFX-EDK *Board Field I/O Pin Connections*

Table 2.2: AXM-VFX-EDK *Board Field JTAG Pin Connections*

AXM-VFX-EDK Front I/O

14-Pin 2mm Double Row JTAG Header			
Pin Description	**Pin**	**Pin Description**	**Pin**
COMMON	1	+3.3V	2
COMMON	3	TMS	4
COMMON	5	TCK	6
COMMON	7	TDO	8
COMMON	9	TDI	10
COMMON	11	Not Connected	12
COMMON	13	Not Connected	14

Table 2.3: AXM-VFX-EDK
Auxiliary I/O Pin Connections

Auxiliary (LVTTL) I/O Pin Connections (SIP)			
SIP 1 (S1)		**SIP 2 (S2)**	
Pin Description	**Pin**	**Pin Description**	**Pin**
AUX Channel 0	1	AUX Channel 8	1
AUX Channel 1	2	AUX Channel 9	2
AUX Channel 2	3	AUX Channel 10	3
AUX Channel 3	4	AUX Channel 11	4
AUX Channel 4	5	Not Available	5
AUX Channel 5	6	Not Available	6
AUX Channel 6	7	Not Available	7
AUX Channel 7	8	Not Available	8

Table 2.4: AXM-VFX-EDK
9- Pin DSUB Connections

9-Pin DSUB Connections		
Pin Description	**Connections**	**Pin**
DCD	Pins 1, 4 and 6 shorted	1
Receive Data	Receive Data	2
Transmit Data	Transmit Data	3
DTR	Pins 1, 4 and 6 shorted	4
Ground	Ground	5
DSR	Pins 1, 4 and 6 shorted	6
RTS	Pins 7 and 8 shorted	7
CTS	Pins 7 and 8 shorted	8
RI	Open connection	9

Non-Isolation Considerations

The board is non-isolated, since there is electrical continuity between the logic and field I/O grounds. As such, the field I/O connections are not isolated from the system. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

3.0 PROGRAMMING INFORMATION

This Section provides the specific information necessary to program and operate the board.

The generic memory space address map for the board is shown in Table 3.1. The actual bit mapping in the individual registers are detailed in the register descriptions later in this manual. Note that the PCIBAR2 from the base PMC module in memory space must be added to the addresses shown to properly access the board registers. Register accesses as 32, 16, and 8-bits in memory space are permitted.

AXM-VFX-EDK MEMORY MAP

Table 3.1: Memory Map

Base Addr+	D31 D16	D15 D00	Base Addr+
0003 ↓ 7FFF	Reserved for base PMC Module[1]		**0000 ↓ 7FFC**
8003	Board Status Register and Software Reset[2]		**8000**
8007	29-0 EDK I/O Register[3]		**8004**
800B	Direction Register EDK Channels 29-0[3]		**8008**
800F	15-0 Digital I/O Register[3]		**800C**
8013	Direction Register Digital Channels 15-0[3]		**8010**
8017	Not Used[4]	Interrupt Enable Differential Ch. 15-8	**8014**
801B	Not Used[4]	Interrupt Type Differential Ch. 15-8	**8018**
801F	Not Used[4]	Interrupt Polarity Differential Ch. 15-8	**801C**
8023	Not Used[4]		**8020**
8027	Not Used[4]		**8024**
802B	Not Used[4]		**8028**
802F ↓ 1FFFFF	Reserved for base PMC Module[1]		**802C ↓ 1FFFFC**

1. This address space is not defined for this module. This space may be used on the base PMC Module. Refer to the base PMC module User's Manual for further information

2. These registers have bits that are reserved for the base PMC module. See the register definition later in this manual for further details.

3. The bits used in these registers varies for each model. Refer to the register descriptions in the following pages for specific module mapping.

4. The board will return 0 for all addresses that are "Not Used".

This memory map reflects byte accesses using the "Little Endian" byte ordering format. Little Endian uses even-byte addresses to store the low-order byte. The Intel x86 family of microprocessors uses "Little Endian" byte ordering. Big Endian is the convention used in the Motorola 68000 microprocessor family and is the VMEbus convention. In Big Endian, the lower-order byte is stored at odd-byte addresses.

BOARD STATUS AND RESET REGISTER

Board Status and Software Reset Register (Read/Write) – (PCIBAR2 + 8000H)

This read/write register is used the issue a software reset, view and clear pending interrupts, and to identify the attached module. It may also provide other functions that are defined by the base board. Writing a "1" to bit 31 of this register will cause a software reset effecting both the PMC base board and the EDK registers. Bits 15 to 13 are used for AXM identification code.

Bits 0 to 7 or this register reflect the status of each of the Differential I/O channels 8 to 15. A **Read** of this bit reflects the interrupt pending status. Read of a "1" indicates that an interrupt is pending for the corresponding differential channel. **Write** of a logic "1" to this bit will release the corresponding differential channel's pending interrupt. Writing "0" to a bit location has no effect, a pending interrupt will remain pending.

BIT	FUNCTION	
0	Differential Channel 8 Interrupt Pending/Clear	
1	Differential Channel 9 Interrupt Pending/Clear	
2	Differential Channel 10 Interrupt Pending/Clear	
3	Differential Channel 11 Interrupt Pending/Clear	
4	Differential Channel 12 Interrupt Pending/Clear	
5	Differential Channel 13 Interrupt Pending/Clear	
6	Differential Channel 14 Interrupt Pending/Clear	
7	Differential Channel 15 Interrupt Pending/Clear	
12-8	Reserved for PMC base board[3]	
15-13	AXM Identification bits[1,2] (Read Only)	
	AXM-D	"001"
	AXM-EDK	"001"
30-16	Reserved for PMC base board[3]	
31	Software Reset (Write Only)	

1. Note that if no AXM module is attached the register will still read "001". It is up to the end user to differentiate if no mezzanine module is attached.
2. All other 3 bit values are reserved for future use.
3. Bit function is defined by the base PMC Module.

This register can be written with either 8-bit, 16-bit, or 32-bit data transfers.

EDK Input/Output Registers (Read/Write) – (PCIBAR2 + 8004H)

DIFFERENTIAL INPUT/OUTPUT REGISTERS

The AXM-VFX-EDK LVTTL channels may be individually accessed via this register at the carrier PCIBAR2 + 8004H. This includes all 30 general purpose LVTTL channels on the AXM-VFX-EDK. Each channel is controlled by its corresponding data bit, as shown in the register mapping table below. Channel input signal levels are determined by reading this register. Likewise, channel output signal levels are set by writing to this register. Note that the data direction, input or output, must first be set via the Differential Direction register at PCIBAR2 plus 8008H.

D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**
Not Used		I/O 29	I/O 28	I/O 27	I/O 26	I/O 25
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**
I/O 23	I/O 22	I/O 21	I/O 20	I/O 19	I/O 18	I/O 17
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**
I/O 15	I/O 14	I/O 13	I/O 12	I/O 11	I/O 10	I/O 9
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**
I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1

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Channel read/write operations use 8-bit, 16-bit, or 32-bit data transfers with the lower ordered bits corresponding to the lower-numbered channels for the register of interest. All input/output channels are configured as inputs following a power-on or software reset. Data-bits 30 and 31 are not used and will return 0 when read. Data bits 0 through 7 in the AXM-D03 module will read back the last data values written to those bits.

DIFFERENTIAL INPUT/OUTPUT REGISTERS

Differential Direction Control Register (Read/Write) – (PCIBAR2 + 8008H)

The data direction (input or output) of the differential channels is selected via this register at the carrier PCIBAR2 + 8008H. This includes the direction of all 30 general purpose LVTTL channels on the AXM-EDK. The direction of each channel is controlled by its corresponding data bit. Data bit use varies depending on the module selected. The bit mapping corresponds to the Differential and EDK I/O Register.

Independent channel direction control is provided for each differential channel. Setting a bit low configures the corresponding channel data direction for input. Setting the control bit high configures the corresponding channel data direction for output.

The default power-up state of these registers is logic low. Thus, all channels are configured as inputs following system reset or power-up. Reading or writing to this register is possible via 32-bit, 16-bit or 8-bit data transfers. Data-bits 30 and 31 are not used and will return 0 when read.

Digital Input/Output Registers (Read/Write) – (PCIBAR2 + 800CH)

DIGITAL INPUT/OUTPUT REGISTERS

Digital CMOS input/output channels may be individually accessed via this register at the carrier PCIBAR2 + 800CH. This includes twelve auxiliary LVTTL I/O on the AXM-VFX-EDK module. Channel input signal levels are determined by reading this register. Likewise, channel output signal levels are set by writing to this register. The data bits are mapped according to the following table. Note that the data direction, input or output, must first be set via the Digital Direction register at PCIBAR2 plus 8008H.

Model	Digital I/O Register Mapping							
	D15	D14	D13	D12	D11	D10	D9	D8
VFX-EDK	Not Used	Not Used	Not Used	Not Used	AUX 11	AUX 10	AUX 9	AUX 8

	D7	D6	D5	D4	D3	D2	D1	D0
VFX-EDK	AUX 7	AUX 6	AUX 5	AUX 4	AUX 3	AUX 2	AUX 1	AUX 0

DIGITAL INPUT/OUTPUT REGISTERS

Channel read/write operations use 8-bit, 16-bit, or 32-bit data transfers with the lower ordered bits corresponding to the lower-numbered channels for the register of interest. All input/output channels are configured as inputs following a power-on or software reset. Data-bits 16 through 31 are not used and will return 0 when read.

Digital Direction Control Register (Read/Write) – (PCIBAR2 + 8010H)

The data direction (input or output) of the digital channels is selected via this register at the carrier PCIBAR2 + 8010H. This includes twelve auxiliary LVTTL I/O on the AXM-VFX-EDK module. The direction of each channel is controlled by its corresponding data bit. The register mapping is the same as the Digital I/O Register. Data-bits 13 through 31 are not used and will return 0 when read.

Independent channel direction control is provided for each digital channel. Setting a bit low configures the corresponding channel data direction for input. Setting the control bit high configures the corresponding channel data direction for output.

The default power-up state of these registers is logic low. Thus, all channels are configured as inputs following system reset or power-up. Reading or writing to this register is possible via 32-bit, 16-bit or 8-bit data transfers.

DIFFERENTIAL INTERRUPT REGISTERS

Interrupt Enable Register (Read/Write) – (PCIBAR2 + 8014H)

The Interrupt Enable Register provides a map bit for each differential channel from 8 to 15. A "0" bit will prevent the corresponding input channel from generating an external interrupt. A "1" bit will allow the corresponding channel to generate an interrupt.

The Interrupt Enable register at the PCIBAR2 + offset 8014H is used to control channels 8 through 15 via data bits 0 to 7. Bits 8 to 15 are not used and will always read as "0".

All channel interrupts are disabled (set to "0") following a power-on or software reset. Reading or writing to this register is possible via 32-bit, 16-bit or 8-bit data transfers. Additional steps may be required to enable interrupts. Refer to the PMC base module's User's Manual for further information.

Model	Interrupt Register Mapping							
	D7	D6	D5	D4	D3	D2	D1	D0
VFX-EDK	I/O 15	I/O 14	I/O 13	I/O 12	I/O 11	I/O 10	I/O 9	I/O 8

DIFFERENTIAL INTERRUPT REGISTERS

Interrupt Type (COS or H/L) Configuration Register (Read/Write) - (PCIBAR2 + 8018)

The Interrupt Type Configuration Register determines the type of input channel transition that will generate an interrupt for each of the eight possible interrupting channels. A "0" bit selects interrupt on level. An interrupt will be generated when the input channel level specified by the Interrupt Polarity Register occurs (i.e. Low or High level transition interrupt). A "1" bit means the interrupt will occur when a Change-Of-State (COS) occurs at the corresponding input channel (i.e. any state transition, low to high or high to low).

The Interrupt Type Configuration register at PCIBAR2 + 8018H is used to control channels 8 through 15 as mapped in the Interrupt Enable Register. For example, channel 8 is controlled via data bit-0. Bits 8 to 15 are not used and will always read as "0".

All bits are set to "0" following a reset which means that, if enabled, the inputs will cause interrupts for the levels specified by the Interrupt Polarity Register.

Channel read or write operations use 8-bit, 16-bit, or 32-bit data transfers. Note that no interrupts will occur unless they are enabled by the Interrupt Enable Register.

Interrupt Polarity Register (Read/Write) – (PCIBAR2 + 801C)

The Interrupt Polarity Register determines the level that will cause a channel interrupt to occur for each of the channels enabled for level interrupts. A "0" bit specifies that an interrupt will occur when the corresponding input channel is low (i.e. a "0" in the differential input channel data register). A "1" bit means that an interrupt will occur when the input channel is high (i.e. a "1" in the differential input channel data register). Note that no interrupts will occur unless they are enabled by the Interrupt Enable Register. Further, the Interrupt Polarity Register will have no effect if the Change-of-State (COS) interrupt type is configured by the Interrupt Type Configuration Register.

The Interrupt Polarity register at the PCIBAR2 + offset 801CH is used to control differential channels 8 through 15 as mapped in the Interrupt Enable Register. For example, channel 8 is controlled via data bit-0. Bits 8 to 15 are not used and will always read as "0".

All bits are set to "0" following a reset, which means that the inputs will cause interrupts when they are logic low (provided they are enabled for interrupt on level).

4.0 THEORY OF OPERATION

This section contains information regarding the hardware of the board. A description of the basic functionality of the circuitry used on the board is also provided. Note that each section does not necessarily apply to every model. Refer to table below to determine the appropriate sections.

MODEL	I/O Type	Interrupts	JTAG Support
AXM-VFX-EDK	30 LVTTL	8 Channels	Yes

LVTTL DIRECT INTERFACE

The AXM-VFX-EDK has a total of 42 (30 General Purpose and 12 auxiliary) channels of LVTTL. These I/O provide a direct connection through the mezzanine connector to the adjoining FPGA. There are no intermediate buffers on the I/O. As such care must be taken to limit overshoot (to 3.6V) and to prevent ESD, or the FPGA on the PMC base board may be damaged.

The I/O on the AXM-VFX-EDK are mapped to simulate the various types of I/O that can be found on the AXM-D series modules. Therefore the same registers can be used to simulate the Field I/O on the AXM-VFX-EDK. The 30 general purpose I/O map to the 30 differential I/O on the AXM-D02, the 22 differential I/O on the AXM-D03, and 30 LVDS I/O on the AXM-D04. The 16 auxiliary I/O map to the 16 differential signal on the AXM-D03. Note that regardless of which AXM-D module is being emulated, the AXM-VFX-EDK I/O are all 3.3V LVTTL.

JTAG INTERFACE

The AXM-VFX-EDK model has a front field I/O Xilinx JTAG header. It readily connects to any compatible Xilinx programming system such as the MULTIPro Tool® or Parallel Cable programming system. In general, the JTAG interface pins connect only to the Xilinx FPGA. See the PMC base board for further information. The JTAG interface is powered by 3.3V.

INTERRUPT LOGIC

Eight Channels in each model can be configured to generate interrupts for Change-Of-State (COS) and input level (polarity) match conditions. The interrupt is released via a write to the corresponding bit of the Interrupt Status/Clear register. The channels enabled for interrupt in the example design are Differential Channels 8 to 15 on the LVTTL Channels 8-15 on the AXM-EDK.

PMC BASE BOARD CONNECTION

The AXM-VFX-EDK and AXM-D series of extension I/O modules are attached to the PMC base board via a high speed 150 pin header. The connector provides power to the extension board and multiple logic connections to the base board. Note that any PMC base board with a re-configurable FPGA will require the pin definitions provided in the EDK to properly operate the AXM-VFX-EDK and AXM-D series boards.

5.0 SERVICE AND REPAIR

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

SERVICE AND REPAIR ASSISTANCE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier/CPU board to verify that it is correctly configured. Replacement of the board with one that is known to work correctly is a good technique to isolate a faulty board.

PRELIMINARY SERVICE PROCEDURE

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at http://www.acromag.com. Our web site contains the most up-to-date product and software information.

WHERE TO GET HELP

Choose the "Support" hyperlink in our website's top navigation row then select "Embedded Board Products Support" or go to http://www.acromag.com/subb_support.cfm to access:

- Application Notes
- Frequently Asked Questions (FAQ's)
- Knowledge Base
- Tutorials
- Software Updates/Drivers

www.acromag.com

An email question can be submitted from within the Knowledge Base or through the "Contact Us" hyperlink at the top of any web page.

Acromag's application engineers can also be contacted directly for technical assistance via telephone or FAX through the numbers listed at the bottom of this page. When needed, complete repair services are also available.

6.0 SPECIFICATIONS

PHYSICAL

Single AXM-VFX-EDK Board

Stacking Height	5.0 mm (0.197 in)
Depth	99.0 mm (3.9 in)
Width	74.0 mm (2.913 in)
Board Thickness	1.62 mm (0.064 in)

Unit Weight (Including all mounting hardware)

AXM-VFX-EDK: 1.44oz (0.0408Kg)

Connectors

- **AXM-VFX-EDK Front Field I/O:** 14-pin, 2mm double row male header (standard Xilinx JTAG header). 34-pin, 0.1" double row header.

Power Requirements			
		TYP[1]	**MAX[2]**
3.3V (±5%)[1]	VFX-EDK	30mA	70mA
5V (±5%)[1]	VFX-EDK	Not Used	

Table 6.1: Power Requirements for Example Design

1. Power source is the base board. Current draw is for AXM module only.
2. Floating or shorted I/O will have higher current draw.

ENVIRONMENTAL

Operating Temperature: 0°C to +70°C

Relative Humidity: 5-95% Non-Condensing.

Storage Temperature: -55°C to 150°C.

Non-Isolated: Logic and field commons have a direct electrical connection.

Radiated Field Immunity (RFI): Complies with EN61000-4-3 (3V/m, 80 to 1000MHz AM & 900MHz. keyed) and European Norm EN50082-1 with no register upsets.

Conducted R F Immunity (CRFI): Complies with EN61000-4-6 (3V/rms, 150KHz to 80MHz) and European Norm EN50082-1 with no register upsets.

Electromagnetic Interference Immunity (EMI): No register upsets occur under the influence of EMI from switching solenoids, commutator motors, and drill motors.

Surge Immunity: Not required for signal I/O per European Norm EN50082-1.

Electric Fast Transient (EFT) Immunity: Complies with EN61000-4-4 Level 2 (0.5KV at field I/O terminals) and European Norm EN50082-1.

Electrostatic Discharge (ESD) Immunity: Complies with EN61000-4-2 Level 3 (8KV enclosure port air discharge) Level 2 (4KV enclosure port contact discharge) Level 1 (2KV I/O terminals contact discharge) and European Norm EN50082-1.

Radiated Emissions: Meets or exceeds European Norm EN50081-1 for class B equipment. Shielded cable with I/O connections in shielded enclosure are required to meet compliance.

SPECIFICATIONS

Mean Time Between Failure: Contact the Factory.

Reliability Prediction

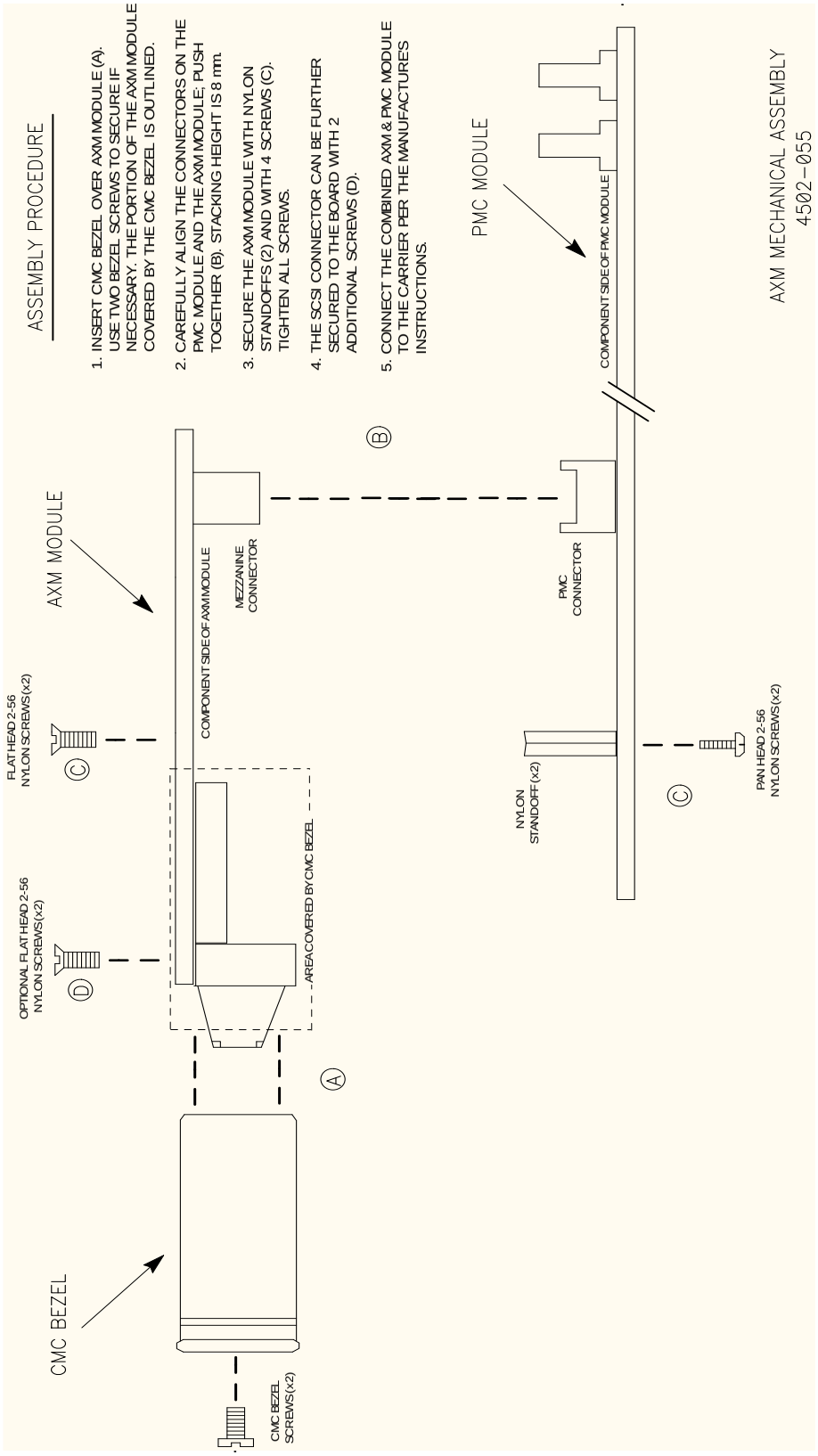
Channel Configuration: 42 Channels (AXM-VFX-EDK) Bi-directional LVTTL signals are independently direction controlled.

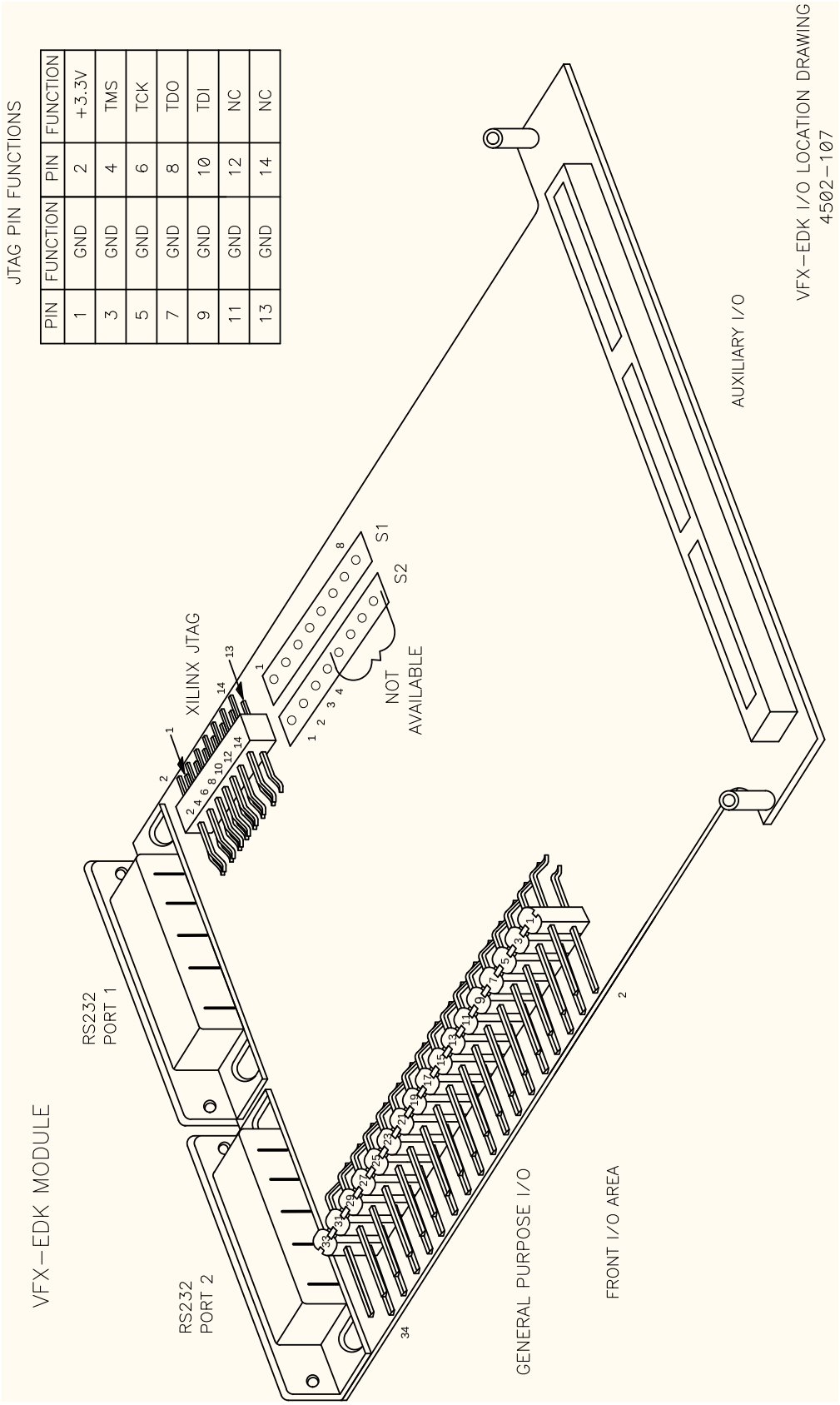
LVTTL I/O

Reset/Power Up Condition: All Digital Channels Default to Input.

LVTTL I/O Characteristics: Due to the direct connections from the Field I/O to the FPGA, all I/O characteristics for LVTTL are determined by the FPGA. Refer to the FPGA documentation for 3.3V signaling for further information.

DRAWINGS


ASSEMBLY PROCEDURE
1. INSERT CMC BEZEL OVER AXM MODULE (A). USE TWO BEZEL SCREWS TO SECURE IF NECESSARY. THE PORTION OF THE AXM MODULE COVERED BY THE CMC BEZEL IS OUTLINED.
2. CAREFULLY ALIGN THE CONNECTORS ON THE PMC MODULE AND THE AXM MODULE; PUSH TOGETHER (B). STACKING HEIGHT IS 8 mm.
3. SECURE THE AXM MODULE WITH NYLON STANDOFFS (2) AND WITH 4 SCREWS (C). TIGHTEN ALL SCREWS.
4. THE SCSI CONNECTOR CAN BE FURTHER SECURED TO THE BOARD WITH 2 ADDITIONAL SCREWS (D).
5. CONNECT THE COMBINED AXM & PMC MODULE TO THE CARRIER PER THE MANUFACTURES INSTRUCTIONS.
AXM MODULE
PMC MODULE
AXM MECHANICAL ASSEMBLY
4502-055
COMPONENT SIDE OF AXM MODULE
MEZZANINE CONNECTOR
COMPONENT SIDE OF PMC MODULE
PMC CONNECTOR
FLAT HEAD 2-56 NYLON SCREWS (x2)
OPTIONAL FLAT HEAD 2-56 NYLON SCREWS (x2)
AREA COVERED BY CMC BEZEL
NYLON STANDOFF (x2)
PAN HEAD 2-56 NYLON SCREWS (x2)
CMC BEZEL
CMC BEZEL SCREWS (x2)
A
B
C
D


VFX-EDK I/O LOCATION DRAWING
4502-107
JTAG PIN FUNCTIONS
PIN FUNCTION PIN FUNCTION
1 GND 2 +3.3V
3 GND 4 TMS
5 GND 6 TCK
7 GND 8 TDO
9 GND 10 TDI
11 GND 12 NC
13 GND 14 NC
VFX-EDK MODULE
RS232 PORT 1
RS232 PORT 2
XILINX JTAG
S1
S2
NOT AVAILABLE
AUXILIARY I/O
GENERAL PURPOSE I/O
FRONT I/O AREA